Amendments to the Claims

1. (*Currently Amended*) A method for producing a fail-safe output signal in case of an open circuit condition of an input pad of a digital circuit unit comprising:

providing a constant switch level in a first inverter stage ~~(10, 18)~~;

providing a variable switch level in the second inverter stage ~~(32, 44)~~ that depends on the signal level of the input pad ~~(28)~~;

comparing the constant switch level of the first inverter stage ~~(10, 18)~~ with the variable switch level of the second stage ~~(32, 44)~~; and

providing an output signal at an output terminal ~~(42)~~ thereof if the switch level of the second stage ~~(32, 44)~~ is greater than the constant switch level; and

decreasing the switch level of the second inverter stage ~~(32, 44)~~ by an additional circuit element (52) connected in series with the second inverter ~~(32, 44)~~,

a defined output being produced irrespective of the open circuit condition of an input pad ~~(28)~~.

2. (*Currently Amended*) A fail-safe circuit for producing a fail-safe output signal in case of an open circuit condition of an input pad of a digital circuit unit, comprising:

a first inverter stage ~~(10, 18)~~ providing a constant switch level;

a second inverter stage ~~(32, 44)~~ providing a variable switch level that depends of the signal level of the input pad ~~(28)~~ and comparing the constant switch level of the first inverter stage ~~(10, 18)~~ with the variable switch level of the second stage ~~(32, 44)~~ and providing an output signal at an output terminal ~~(42)~~ thereof if the variable switch level of the second stage ~~(32, 44)~~ is greater than the constant switch level; and

an additional circuit element ~~(52)~~ connected in series with the second inverter ~~(32, 44)~~ for decreasing the switch level of the second inverter stage ~~(32, 44)~~.

3. (*Currently Amended*) The circuit of claim 2, wherein the first inverter stage ~~(10, 18)~~ is a transistor stage, and wherein the gate electrodes ~~(14, 22)~~ and the drain electrodes ~~(16, 20)~~ of the transistors of the first inverter stage ~~(10, 18)~~ are connected to each other.

4. (*Currently Amended*) The circuit of claim 2, wherein the second inverter stage ~~(32, 44)~~ is a transistor stage, and wherein the gate electrodes ~~(34, 48)~~ of the transistors of the second inverter stage ~~(32, 44)~~ are connected to each other and wherein the drain electrodes ~~(40, 46)~~ of the transistors are connected to each other.

5. (*Currently Amended*) The circuit of claim 2, wherein the gate electrodes ~~(34, 48)~~ of the second inverter stage ~~(32, 44)~~ are connected to the gate electrodes ~~(14, 22)~~ of the first inverter stage ~~(10, 18)~~.

6. (*Currently Amended*) The circuit of claim 2, wherein the input terminal ~~(28)~~ is connected to a source electrode ~~(36)~~ of the second inverter stage ~~(34, 48)~~.

7. (*Currently Amended*) The circuit of claim 2, wherein the output terminal ~~(42)~~ is connected to a drain electrode ~~(40, 46)~~ of the second inverter stage ~~(32, 44)~~.

8. (*Currently Amended*) The circuit of claim 2, wherein the additional circuit element ~~(52)~~ is a transistor in saturated mode.

9. (*Currently Amended*) The circuit of claim 2, wherein the additional circuit element ~~(52)~~ is a transistor in saturated mode where the gate ~~(56)~~ of the transistor ~~(52)~~ is connected to the VCC and the source ~~(58)~~ is connected to ground, the defined signal being a high level signal.

10. (*Currently Amended*) The circuit of claim 2, wherein the additional circuit element ~~(80)~~ is a transistor in saturated mode where the gate ~~(84)~~ of the transistor is connected to ground and the source ~~(82)~~ is connected to VCC, the defined signal being a low level signal.

11. (*Currently Amended*) A digital circuit unit comprising an input terminal, a pull-up stage ~~(2)~~, a fail-safe stage ~~(4)~~, a signal processing stage ~~(6)~~ and an output terminal,

wherein the fail-safe stage ~~(4) comprises the features of claims 2 to 10.~~ comprises the features of claim 2.